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a	Initial version		DRC	

CUSTOMER User Manual Rev. 1.0

CPiA 1.5 + 6409 USB Camera Chipset Reference Design Manual

The VISION CPiA 1.5 + VV6409 USB Reference Design allows customers to build a production ready USB Camera for PC video capture applications.

The camera is based upon VISION's VV6409 CMOS CIF resolution colour sensor and the VV0670 CPiA 1.5 (colour Processor Interface ASIC).

This ASIC performs the colour processing, and compression of the video data and also contains the USB interface. The only extra components required are a DRAM for the framestore, and suitable power supply components.

The reference design camera consists of two PCBs. A head PCB and an interface PCB. The sensor and lens assembly are mounted on the head PCB and CPiA and other supporting electronics are mounted on the interface PCB.

It is possible to implement the design as a single PCB.

This Document is a high level description of the Camera design. It contains an explaination of the electronics, and some guidelines for PCB layout and system design.

For more detailed information on the VISION custom ICs please see the relevent VISION Data sheets

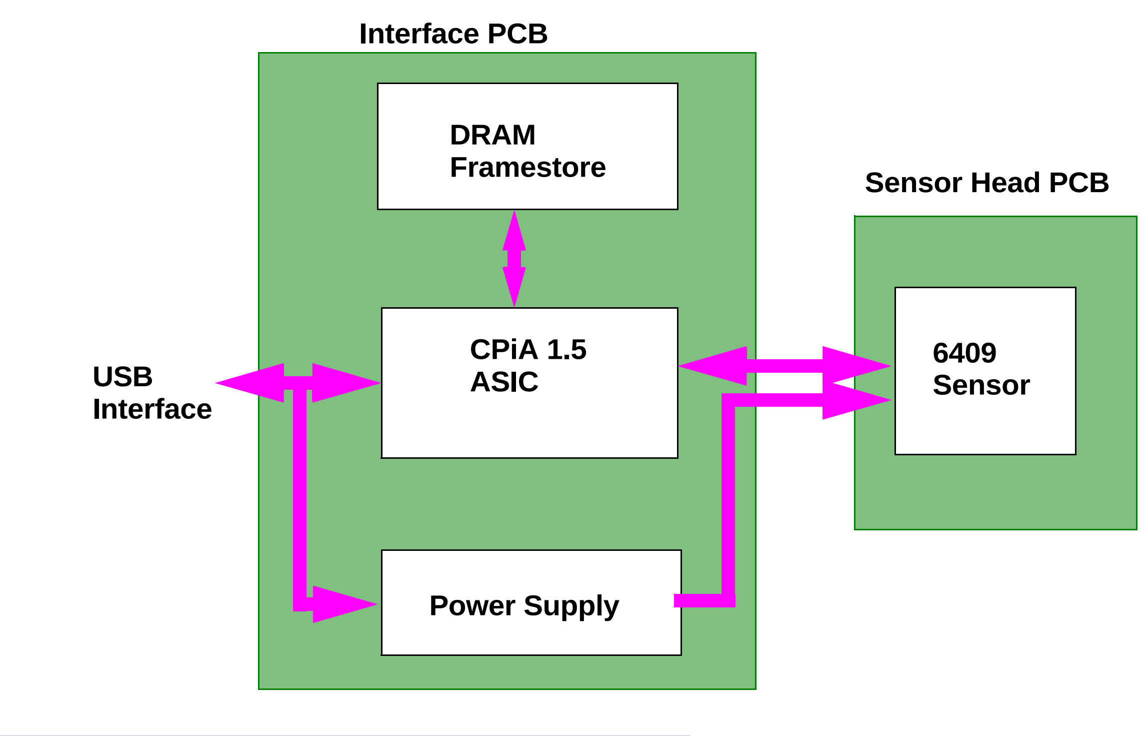
KEY FEATURES

- Full Reference Design for USB Camera
- Supports 2-layer PCB design
- EMC test ready
- Compliant with USB Specification v1.0
- Production-ready Win95 and Win98 drivers
- Isochronous data transfer mode
- ECP Parallel Port mode available

Reference Data

- Reference Design Manual
- Schematics
- PCB Gerber files
- Sensor footprint drawing
- Cable drawings
- Bill of Materials (BOM)
- EMC shield design
- Chipset Datasheet

System Block Diagram



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1. Introduction

This reference design manual describes a complete production-ready reference design for a USB camera using the VISION CPiA1.5 and VV6409 devices.

It includes an overview of the system design, a detailed description of the electronics, the parts list for the design, and also considerations for PCB layout.

For additional information refer to the relevant datasheets for the VISION devices, and also the reference data listed.

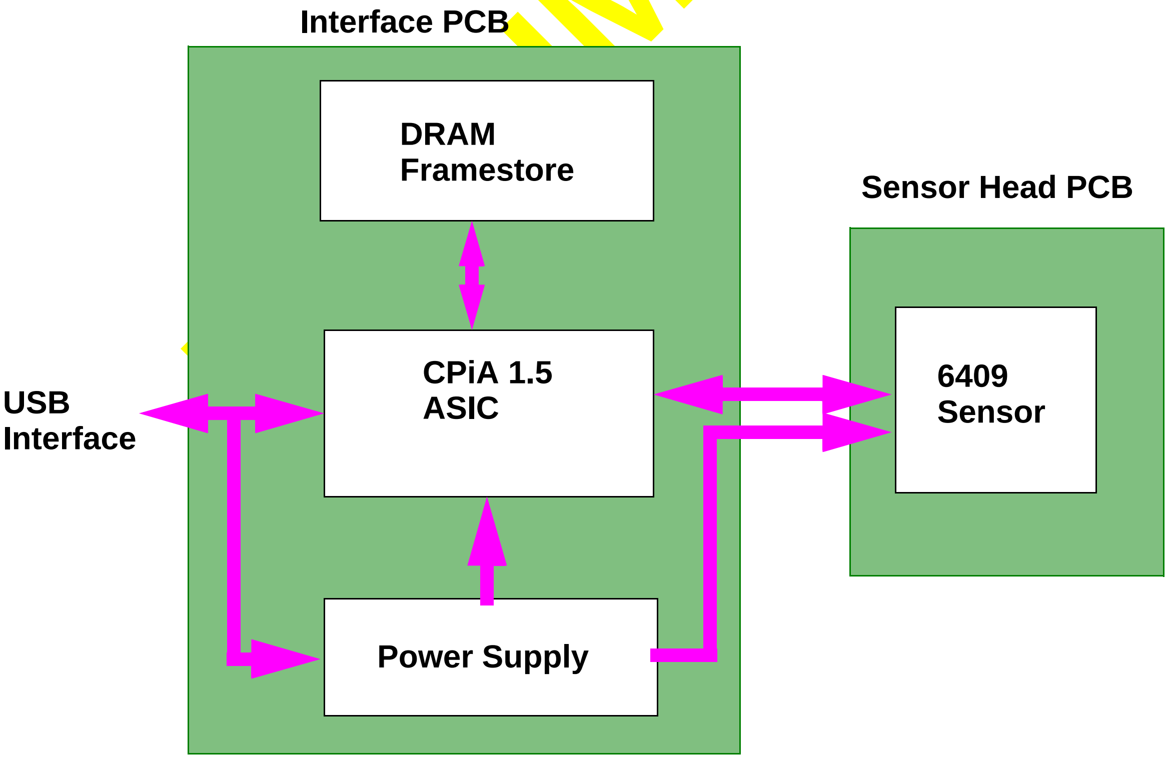
1.1 System Overview

The USB camera design comprises 3 main functional blocks

- The Sensor and support circuit
- The CPiA ASIC and DRAM framestore
- The Power supply circuit

In the reference design these three blocks are split over two PCB's for design convenience, but this is not essential. If a single PCB design is being considered, please check the appropriate section in the PCB Layout guidelines.

Figure 1 : Block Diagram of CPiA 1.5 + 6409 USB Camera



1.2 Sensor and support circuit

The VV6409 sensor requires a minimum of support circuit to allow it to operate. The design includes an serial EEPROM for use for Pixel Defect Correction. If Pixel Defect Correction is not being implemented this part can be ommitted.

1.3 CPiA and DRAM

The Colour Processor Interface ASIC (CPiA) digital video processor is the heart of the camera. CPiA accepts raw digital data from the CMOS sensor and transfers the resulting YUV video data to the USB host at up to 30 frames per second.

The CPiA ASIC contains the following functions:

- Sensor Interface - generating the sensor clock, controlling the sensor via the serial bus
- Video Processor - this converts the raw sensor data into YUV colour data
- Video Compressor - the compressor uses the external DRAM to perform inter-frame compression on the video data.
- USB Interface - the compressed data is transmitted to the PC via the USB interface
- System Management - co-ordinates system operation, responding to host requests and commands as well as performing automatic camera exposure control and colour balance.

An external 4Mbit or 16Mbit EDO 60nS DRAM is used to store both the uncompressed CIF or QCIF image and the compressed USB image that is waiting to be transferred over the USB data bus. The larger devices can be used if they are more economic, but most of the device will be unused.

1.4 Power Supply Circuit

The USB camera design has a fairly sophisticated power supply design to accomodate the Power Management requirements of the USB specification. As well as providing 3.3V to power the CPiA and the DRAM, it also allows different parts of the design to be powered down separately.

There is an option to include a DC - DC switcher circuit to allow the camera to be used as a low-power USB device (i.e. connect via a bus-powered hub).
Please contact VISION for more information on this option.

2. Electronics Design

The following sections discuss the design in detail. They should be read in conjunction with the schematics for the CPiA 1.5 + VV6409 USB Camera Reference Design, which are available separately.

The reference design is split into two Schematics: The Camera Head Board Schematics, and the Interface Board Schematics

2.1 Camera Head Board Schematics

The camera head schematics contain the VISION VV6409 sensor, the support circuit and the Serial EEPROM for defect correction.

VISION sensors are packaged in two Package types, LCC and BGA, and VISION recommend that any sensor PCB layout includes the appropriate pinout for both packages. A recommended PCB layout is available that contains the BGA footprint inside the LCC footprint to minimise board area and ensure optical alignment. The pinouts for both options are shown on pages 1 and 3 of the schematics.

The following items are optional components and should be treated as detailed below. For all other component information, please consult the Bill of materials section.

Component	Page	Comment
C15 C16, R5, J3,	1	NOT FITTED - these components are not required as the CPiA 1.5 does NOT support Audio.
J4	1	NOT FITTED - J4 is a test socket and is not required
R10	1	NOT FITTED - R10 is not required for normal operation
IC3	1	NOT FITTED (unless defect correction is being used) NOTE: VISION recommends that the footprint for IC3 is included on all PCB designs, in case defect correction is required in future.
R1	2	SHORTED OUT - this component is not required and should be replaced by a track on the PCB.
U19	2	NOT FITTED - this regulator is not required for the USB camera design.
IC2	2	NOT FITTED - this component is not required.
R2		SHORTED OUT - this component is not required and should be replaced by a track on the PCB.
R4	2	NOT FITTED - this component is not required.
C19	2	NOT FITTED - this component is not required.

Table 1 : Camera head optional components

2.2 Interface Board Schematics

The interface Board contains the CPiA ASIC and support circuit, the DRAM and the Power supply and USB interface.

These blocks are shown on page 1 of the schematics.

2.2.1 Page 2 - CPiA Block

This page contains the CPiA ASIC, the camera head connector, and the clock circuits.

2.2.1.1Clocks and Crystals

Three clocks are used by the system.A low frequency 400Hz 555 based clock for low power suspend mode. A 48MHz clock for Driving the USB interface and a 14.318MHz for driving the internal functions of the camera. CPiA provides a clock for the camera head derived from the above clocks.

The two crystals are shown on this page. The circuitry around X2 is required because the X2 is a third overtone Crystal. The 555 timer circuit is also shown, and this circuit generates the 400Hz clock required by CPiA.

2.2.1.2Camera Head Interface connector

J1 is the connector for the interconnect cable going to the head PCB. The passive devices clustered around the connector and R26,R27,C75 and C73 are required to condition signals before they are sent over the interconnection cable.

2.2.1.3Optional Components

The following items are optional components and should be treated as detailed below. For all other component information, please consult the Bill of materials section.

Component	Page	Comment
F2	2	SHORTED OUT - this component is not required and should be replaced by a track on the PCB.
R10, R9, R15	2	SHORTED OUT - this component is not required and should be replaced by a track on the PCB.
R3, R5, R7, R8	2	NOT FITTED - these components are not required for normal operation
R25	2	SHORTED OUT - this component is not required and should be replaced by a track on the PCB.
R23, R24, R28	2	These components select debug options on the CPiA and are not needed. Pins

Table 2 : Camera head optional components

Component	Page	Comment
C4	2	NOT FITTED - C4 is not required for normal operation
C86	2	NOT FITTED - C86 is not required for normal operation
C62, C63, C58	2	NOT FITTED - These are spare decoupling capacitors and they are not required for normal operation
R15, R16, R18, Q7, J3	2	NOT FITTED - These components are for driving a high brightness LED and are not normally fitted[1]
J2	2	NOT FITTED - J2 is a test connector[2] and is not required for normal operation

Table 2 : Camera head optional components

1. If the LED is a low power device(<2.5mA) R16 should be populated and the device will be driven by CPiA directly. If a normal or high brightness LED (<12mA) is to be used then R18, Q7 and R19 should be populated. The LED will light when the camera is capturing video.
2. J2 is a RS232 test connector. If pin3 (RXD) is held low on camera power up, then the camera will go into self diagnostic mode. The result of the diagnostics will be output via this port. Details of the break out required to interface to this connector can be found in a separate document.

For more information on CPiA please see the CPiA Data Sheet.

2.2.2 Page 3 - System Memory

This page has the DRAM memory that is used as a framestore by the CPiA ASIC.

The device is a 60nS EDO DRAM. Details for the exact specification of the DRAM can be found in the CPiA data sheet. The DRAM can be a 256Kx16 DRAM or a 1Mx16 DRAM. If a 256Kx16 DRAM is to be used then populate R102 and R103, else populate with a 1Mx16 DRAM and R104. The extra memory in the 1Mx16 DRAM is not used by the CPiA chip, however in time it may be more cost effective to populate the larger memory option.

2.2.3 Page 4 - Power Supply and USB Interface

The USB camera is powered from the USB interface, which supplies nominal +5v.

The USB connection is either via a PCB mounting type B USB connector (J8) or via a fixed cable connection (J4). The D+ and D- signals connect directly to the CPiA ASIC.

2.2.3.1Power Supply control

The USB specification requires that the camera controls the power surge into the camera when it is hot plugged into a USB network. This is achieved by monitoring the current consumed by the camera. This is carried out by Q4, R6 and R12. When the voltage across R6 increases to 500mA then Q4 starts to switches on. The voltage at the collector of Q4 then starts to rise. This signal is used to limit the current consumption of the camera in two ways. Firstly Q2 starts to turn off restricting the current that the circuit can draw. Secondly Q5 starts to turn on which stops Q6 from turning on and therefore the switcher is prevented from pulling current from the supply.

A linear regulator is used to derive 3.3v for the CPiA and the DRAM

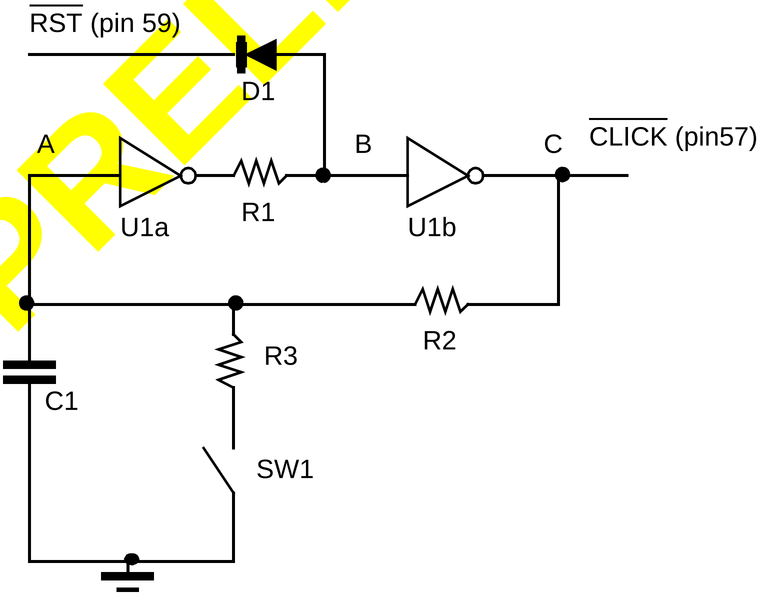
On command from the CPiA ASIC the Power supply control will power down parts of the camera so that the camera can meet the USB standby mode power consumption requirements(see the USB Specification Ver 1.0 for more details).

A FET Q3 is used to switch the 3V3A supply to the DRAM using the $\overline{\text{LOPOW}}$ signal from the CPiA ASIC. Another FET Q6 and two transistors, Q1 and Q5 are used to switch the sensor power VCCA, again using the LOPOW signal. (The two transistors are needed to drive the FET to 5v to turn it off properly.)

2.3 Snapshot button control

The CPiA 1.5 supports the connection of a momentary action button for use as a snapshot button for still image capture. This button input is encoded into the frame header and can be interrogated by an application via the Private Interface to the VISION camera driver. (For more information about the driver Private Interface please contact VISION)

The following additional circuit is required to support the snapshot control. It provides hardware debounce for the switch.


$\overline{\text{RST}}$ (pin 59)
D1
A
U1a
R1
B
U1b
C
$\overline{\text{CLICK}}$ (pin57)
R2
R3
C1
SW1

Part	Description
R1, R2	Resistor 10K

Part	Description
R3	Resistor 100R
U1	74LS04 Hex Invertor (or equivalent)
D1	1N1418 Signal Diode (or equivalent)
C1	Capacitor 10nf ceramic
SW1	Switch - normally open momentary action

2.3.1 Circuit Description

The circuit is designed to work with active low signals and is designed to provide positive feedback to a high or low voltage held on a capacitor. The feedback paths are high impedance and can be over ridden by lower impedance signals.

In use point B is at the opposite voltage to points A and C, so if point A is high then B is low and C is high, C being high keeps A high.

The circuit will boot with A low, due to the capacitor. Before the circuit can be used it must be reset. This is acheived by pulling the $\overline{\text{RST}}$ signal low. When $\overline{\text{RST}}$ is low it overcomes the drive of the gate though the 100K resistor and point B goes low. Therefore point C goes high. The capactor starts to charge though the second 100K resistor and after 100mS (the time constant of 100nF and 10KOhms) point A goes high. $\overline{\text{RST}}$ can now be released as point B is now held low by the feedback though the gate.

When the user wishes to take a picture, they will press a normally open switch closing the contacts. This will discharge the capacitor though the 100R resistor. Point A will go low,point B will go high and point C ($\overline{\text{CLICK}}$) will go low, indicating that the switch has been pressed. The circuit state is kept if the switch is released by the feedback in the circuit.

When required the circuit can be reset, as above, by pulling $\overline{\text{RST}}$ low.

2.3.2 Operation

The snapshot button feature of the CPIA device, and Driver support for it, operate as follows:

When the push button is pressed the external circuit latches indicating that the button has been pressed. This is connected to the CLICK pin of CPIA 1.5.

After each frame is uploaded the driver checks the state of the button latch input. If it detects the button has been pressed it records this fact, and then clears the push button latch via the $\overline{\text{RST}}$ output on CPIA 1.5.

At any time the application may ask the driver, via the private interface, if any <button pressed> events have been detected, since the last time that the application asked the driver. Requesting this information from the driver causes the driver internal <button pressed> record to be reset.

The application is only informed of the fact that a <button pressed> event
has been detected. It can not determine how may, or duration of the presses,
actually occured since it last asked the driver.

NOTES

- Because of the external latch, very short push button events can be detected reliably.
- Because the driver effectively "latches" it's detection of push button events the application can poll the driver at any rate it wants without missing a push button event.
- Before the push button can be used the application must request that the driver start checking the push button state each frame. There is a performance hit for doing the button checking operation, so it is not enabled by default.
- Only "push button pressed" events are recorded by the driver. There is no support for "button down", "button up" style of events.
- There is currently no callback mechanism for the driver to directly inform the application of a button press event.

2.4 General Purpose Input and Output signals

The CPiA 1.5 device has spare Input and Output pins that can be used for general purpose I/O and controlled from the driver via the Private Interface. This allow additional features, not previously envisaged, to be added to the camera and controlled from application software on the PC.
(For more information on the Driver Private Interface please contact VISION.)

In USB mode the following parallel port pins can be used in addition:

H_STROBE (Input)
H_AUTOFD (Input) I
H_FAULT (Output)
H_INIT (Input)I
H_ACK (Output)
H_BUSY (Output)
H_PERROR (Output)
H_SELECT (Output)

NOTE: If these signals are being used as I/O in USB mode it is necessary to pull the H_SELECTIN pin to 0V, in order to prevent the ASIC entering Parallel Port mode on startup.

3. Bill of Materials

3.1 Camera Head Board Bill of Materials (BOM)

The following parts list is for the Camera Head PCB.

Description	Manf	Part No.	Value	Circuit Ref.	Quan	Comments
PCB 4 Layer	Top Search	PMG020APPCVSN			1	
Vision VV6409 Sensor 48-pin BGA	Vision			IC1	1	
Vision VV6409 Sensor 48-pin LCC	Vision			IC1		Alternative
Serial E^2PROM 8-pin SOIC	Microchip Exar Xicor	24LC01B/P XL24C01AF X24C01AS		IC3	1	
Ceramic Cap 0603 25V/Y5V	Murata	GRM39Y5V104Z25500PT	100nF	C5,C6,C9, C10,C11, C12,C13, C14, C29	9	
Ceramic Cap 0805 25V/Y5V	Murata	GRM40Y5V104Z25PT GRM40Y5V104Z50PT	100nF	C1,C2, C7,C8,	4	
Ceramic Cap 0603 16V/Y5V	Murata	GRM39C0G221J50PT	220pF	C32, C33	2	
Electrolytic Cap 25/35V 20%	Nichicon	UMA1E47MDA UMA1V047MDA RT-025MUS4R7MR	4.7uF	C3	1	USE MINIATURE RADIAL 5mm high
Electrolytic Cap 16V 20%	Towa Nichicon	RT-016MU100MR USA1C100MCA	10uF	C4	1	USE MINIATURE RADIAL 7mm high
Electrolytic Cap 16V 20%	Towa Nichicon	RT-016MUS100M UMA1C100MDA	10uF	C24	1	USE MINIATURE RADIAL 5mm high
Tant Cap 4V	AVX	TAJA106M006R TAJA106M004R	10uF	C25	1	TYPE A CASE
Electrolytic Cap 10V ±20% Case 5x7mm	Nichicon Nippon Chemi-Con	USA1A330MDA SRA33/10	33uF	C26	1	
Resistor 0603 1/16W ±5% (or better)	Hokuriku AVX/ Kyocera Rohm Philips Kamaya	CJ-1/16-0R0-JV CR10-0R0-J-T MCR03-EZH-J-0R0 0603 RC-21 RMC-1/16-ORO-J-TP	0R	R2	1	
Res. 0805 1/8W 5%	Rohm Philips Hokuriku	MCR10EZHJ000 RC-11 CR-1/10-0R0-JV	0R	R1	1	
Res. 0603 5% 1/10W	Rohm Hokuriku	MCR03-EZH-J-330 CR-1/16-330-JV	33R	R3	1	
Res 0603 5% 1/10W	Hokuriku AVX/ Kyocera Rohm Phillips Kamaya	CR-1/16-222-JV CR10-222-J-T MCR03-EZH-J-222 0603 RC-21 RMC-1/16-222-J-TP	2K2	R6,R7	2	
Res 0603 5% 1/10W	Rohm	MCR03-EZH-J-203	20K	R9	1	
Ferrite 0603	Murata	BLM11A102SPT		I2,I4,I6,I8	4	1KΩ @100MHz DCR 0.7Ωmax

3.2 Interface Board PCB Bill of Materials (BOM)

The following parts list is for the Camera Head PCB.

Description	Manf	Part No.	Value	Circuit Ref.	Quan	Comments
PCB - 2 layer	Top Search	PMG019AUSBVSN			1	61mm×60mm approx
Ceramic Cap 0603 16V +80/-20% Y5V (or better)	Murata	GRM39Y5V104Z25500PT	100nF	C1, C5, C6, C7, C11, C14, C17, C23, C56, C59	10	
Ceramic Cap 0603 16V +80/-20% Y5V (or better)	TDK Murata	C1608Y5V1H224KT GRM39Y5V224Z16	220nF	C3	1	
Ceramic Cap 0603 16V ±5% NPO (or better)	TDK Murata AVX/ Kyocera	C1608COG1H470JT GRM39COG470J50-500PT CM105CG470J50AT	47pF	C65	1	
Ceramic Cap 0603 16V ±10% COG (or better)			470pF	C8, C15, C16, C58, C61,	5	Note COG only to be used
Ceramic Cap 0603 16V ±5% NPO (or better)	TDK Murata	C1608COG1H100JT GRM39C0G100D50	10pF	C66, C67	2	
Ceramic Cap 0603 16V ±10% X7R (or better)	TDK Murata	C1608X7R1H152KT GRM39X7R152K50PT	1.5nF	C85	1	
Ceramic Cap 0603 16V ±5% NPO (or better)	TDK Murata AVX/ Kyocera Taiyo Yuden	C1608COG1H220JT GRM39COG220J50PT CM105COG220J50AT UMK107CH220J	22pF	C64	1	
Ceramic Cap 0603 16V ±5% NPO (or better)	TDK Murata AVX/ Kyocera	C1608COG1H101JT GRM39COG101J50PT CM105CG101J50AT	100pF	C73,C75	2	
Ceramic Cap 0603 16V +80/-20% Y5V (or better)	AVX/ Kyocera Murata	CM105Y5V103Z50AT GRM39Y5V103Z50	10nF	C20	1	
Ceramic Cap 0805 16V ±5% NPO (or better)	TDK Murata AVX/ Kyocera Rohm	C2012COG1H102J GRM40C0G102J50PT CM21CG102J50VAT MCH215A102JK	1nF	C44	1	
Ceramic Cap 0805 16V ±20% Y5V (or better)	TDK KEMET	C2012Y5V1C105Z C0805C105Z4VAC	1uF	C13, C62, C57	3	May need to add further suppliers
Aluminum Electrolytic Cap 6.3V ±20%	Towa Nichicon Samsung	RT-6R3MU101MR USA0J101MCA SSM100/6.3	100uF	C29, C84	2	
Ferrite 0805				F1,F3,R4	3	300Ω @100MHz D 0.1Ωmax
3V3 DRAM 256K x 16 60ns (or faster) 40SOJ400MIL				IC5	1	EDO page mode
CPIA 100PQFP	TSMC	TM5322A-NBP3		IC7	1	Custom Gate Array
General Purpose Timer	Harris NS	ICM7555CBA LMC555CM		IC6	1	
Linear Regulator	Motorola Motorola Ricoh Torex	MC78LC33HT1 MC78FC33HT1 RH5RL33AA XC62FP3302PR		IC4	1	Higher drop out voltage spec part (LC) OK for this design SOT89
General Purpose Transistor	Philips Motorola	BCW60A BCW60B		Q1	1	
General Purpose Transistor	Philips Motorola	BCW61A BCW61B		Q4, Q5	2	
Power MOSFET SOT-23	Temic	Si2301DS-T1		Q2, Q3, Q6	3	
Inductor	Sagami	C2520C-2R2K	2.2uH	L4	1	

Description	Manf	Part No.	Value	Circuit Ref.	Quan	Comments
Resistor 0603 1/16W ±5% (or better)	Rohm Hokuriku Kamaya	MCR03-EZH-J-104 CR-1/16-104-JV RMC-1/16-104-J-TP	100K	R1,R21, R67, R74	4	
Resistor 0603 1/8W ±1% (or better)	Rohm	MCR03-EZH-J-1R2	1R2	R6	1	
Resistor 0603 1/8W ±5% (or better)	Rohm	MCR03-EZH-J-103	10K	R2, R20	2	
Resistor 0603 1/8W ±5% (or better)	Hokuriku AVX/ Kyocera Rohm Philips Kamaya	CR-1/16-472-JV CR10-472-J-T MCR03-EZH-J-472 0603 RC-21 RMC-1/16-472-J-TP	4.7K	R11, R12, R24, R24, R26, R27,	6	
Resistor 0603 1/8W ±5% (or better)	Rohm	MCR03-EZH-J-152	1.5K	R49	2	
Resistor 0603 1/8W ±5% (or better)	Rohm	MCR03-EZH-J-240	24R	R50,R51	2	
Resistor 0603 1/8W ±5% (or better)	Rohm Hokuriku Kamaya	MCR03-EZH-J-105 CR-1/16-105-JV RMC-1/16-105-J-TP	1M	R13, R65	2	
Resistor 0603 1/8W ±5% (or better)	Rohm	MCR03-EZH-J-511	510R	R66	1	
Resistor 0603 1/16W ±1% (or better)	Rohm	MCR03-EZH-F-185	1.8M	R17	1	
Resistor 0603 1/16W ±5% (or better)	Hokuriku AVX/ Kyocera Rohm Philips Kamaya	CJ-1/16-0R0-JV CR10-0R0-J-T MCR03-EZH-J-0R0 0603 RC-21 RMC-1/16-ORO-J-TP	0R	F2, R9, R10, R15, R25, R102, R103	7	
Resistor 0603 1/16W ±5% (or better)			33R	R101	1	
Adhesive Spacer	Wing Fung	5R200170			2	Place between: X1 + X2 and PCB
Crystal HC-49/U	ACT	BTB1431A-A 30/50/10/30	14.318 MHz	X1	1	Freq. 14.31818MHz
Crystal HC-49/U	ACT	BTB4800A-CM 30/50/10/30/3rd	48MHz	X2	1	3rd overtone

4. PCB Layout Considerations

The following sections should be studied before implementing a PCB layout for the USB Camera reference design.

4.1 Reference Design

The reference Design PCB is a two layer PCB. One of the layers is dedicated to a ground plane, with as few tracks in it as possible, and all kept as short as possible. The other plane is used for power and signal traces.

L1, C84 and IC2 all have multiple footprints, L1 allows 5mm and 6mm inductors to be used. C84 can be a surface mount or a though hole capacitor. IC2 can be a three or 5 pin device. The Crystals cans are not grounded in the reference design.

4.2 PCB Design Layout Guidelines

The design is the PCB layout should follow normal rules. The following points should also be considered when designing the PCB to reduce EMC.

The CPiA / DRAM (IC7/IC5) interface is a source of emissions and traces should be kept as short as possible. The clock traces are another source of noise and should be kept as short as possible. (ie signals connected to IC5 pins 2 3 4 5 6 7 8 9 10 13 14 16 17 18 19 29 23 24 25 26 27 28 29 30 31 33 34 35 36 37 38 40 41)

The Clock and DRAM circuit should be kept away from the interface cable connector J1 and the USB connector J8. Noise injection from the interface cable to the USB cable has been observed during EMC testing. This resulted in the dual ferrites on the interface cable. This maybe avoided by reducing the power plane coupling between the connectors. (ie all signals to X2, R67, R101, L4, C66, C67,C85,X1, C64, C65, R66, R65

4.3 Dual Footprint sensor drawing

The Dual footprint drawing for the Reference Design is available separately from VISION.

4.4 PCB Gerber files

The gerber files for the Reference Design are available separately from VISION.

5. Mechanical/System design

5.1 Cables

A shielded cable is used to connect the Camera head PCB and the Interface PCB.
A Drawing of the cable assembly is available separately from VISION.

The interconnect cable shield is connected to the top can at the Video processor board side. At the camera head side it is connected to the Head PCB.

5.2 Shielding Cans

To conform with the current EMC regulations, two shielding cans have been fitted to the camera, it is suggested that these cans or similar shielding is fitted in order to achieve EMC compliance.

Drawings of the Shielding cans are available separately from VISION.

5.3 EMC

The VISION camera has passed EMC compliance testing when cased in VISION Plastics. This testing will have to be repeated for any custom design. The length and shielding of the interconnecting cable has been found to be critical to a successful design, the length should be kept to a minim. The cable should have a good braid and foil shield to minimize radiation from the camera. If custom shielding is to be used, it is suggested that the shielding encases as much of the two PCBs and interconnecting cable as possible. Minimisation of the interconnecting cable aperture is a useful action to minimise the EMC problems.

If a tethed cable rather than type B USB connector is to be used, it will be critical to a successful design that the cable is well shielded where it enters the camera housing. All EMC testing has been done with a type B USB connector. VISION recommend the use of this type of connector.

6. Software

The following software is available for use with this reference design:

Software	Available	Comment
Video for Windows (VFW) driver for win95/win98	now	This is the standard driver for video capture It can be customised for specific product naming etc. An OEM Pack is available for those wanting to make more significant modifications to the driver look and feel.
TWAIN Driver	now	This allows the VFW driver to be used as a still image capture device in any TWAIN compliant graphics application.
USB Driver Private Interface	now	Documentation is available for the Private Interface to the USB driver, that allows other software applications to directly control the Camera.
CamTest applet	now	This applet lets the user or support staff quickly test the enumeration and function of the USB camera
USBfix patch	now	This patch fixes an enumeration problem with some PC's where the PC will not boot with the camera attached.
Directshow driver for win98/ win2000	In development	This driver uses the DirectMedia interface of Directshow for win98 and win2000
USB driver for Apple Mac USB with OS8.5+	In development	This driver will allow the camera to work on USB-equipped Macs, e.g. iMac.

Table 3 : Software for Reference Design

For more information on any of these software elements please contact VISION.

7. Reference Data

The following additional documentation is available from VISION and it is recommended that it is consulted before starting a design based on this chipset.

Document	Description
CPiA 1.5 Datasheet	This document contains detailed information about the CPiA 1.5 ASIC
VV6409 + CPiA 1.5 Chipset Datasheet	This document contains chipset-level details of both parts and provides sufficient information to design in these parts, in conjunction with the Reference Design Manual (NOT YET AVAILABLE)
Camera Head Schematics	A PDF version of the scematics for this reference design
Interface PCB shematics	A PDF version of the scematics for this reference design
Camera Head Gerber files	The gerber files for the Reference Design Camera Head PCB. A PDF version is available for those unable to read raw gerber files.
Interface PCB shematics	The gerber files for the Reference Design Interface PCB. A PDF version is available for those unable to read raw gerber files.
VV6409 Dual footprint Drawing	This is a PDF drawing of the recommended dual BGA and LCC footprint for the VISION VV6409 sensor.
Shielding Can drawings	These are PDF drawings of the recommended shielding cans for the reference design.
Interface Cable assembly drawing	This is a PDF drawings of the interface cable for the reference design.

Table 4 : Additional Reference Documentation

8. Ordering details

Part number	Description
VV6409B002	BGA packaged CIF Image Sensor
VV0670P002	VISION Colour Processing and Interface ASIC 1.5 (‘CPiA 1.5’)
REF-CPiA1.5	Reference Design Kit for VISION CPIA1.5 + VV6409

Table 5 : Ordering details

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